REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

Claims 14-20 are pending in this case. Claims 14, 15, and 16 have been amended to more clearly define the scope of the claimed invention.

Claims 14-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Arima, in view of Khandros and Dalal, and further in view of DiStefano, et al. (U.S. Patent No. 5,367,764). Applicant respectfully traverses the rejection.

Claim 14 includes the feature of "applying radiant energy to said interposer and then aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer." As pointed out in Applicant's response to the last Office Action, The Arima, Khandros, and Dalal references fail to teach or suggest such a feature. The Examiner has now cited DiStefano for its method of making a multi-layer circuit assembly, including a step of heating interposer materials until they reach a fluid state prior to assembly with circuit panels. However, Applicant respectfully submits that the cited combination of references lacks a suggestion in any of the references for a combined teaching of the claimed invention. For example, DiStefano's teaching of a method of making a multi-layer circuit assembly composed of circuit panels and interposers does not involve a semiconductor device (whether in chip *or* wafer form) as do the other references. The skilled artisan would therefore have received no motivation from DiStefano or the other references to apply radiant energy to an interposer prior to alignment with a semiconductor wafer. As mentioned in a prior response, Arima pertains exclusively to semiconductor chips, not wafers. Khandros was cited for its

teaching of a "planar array of solder balls." However, Khandros's solder 52' is on pads 48 on interposer 42, not on pads on the semiconductor chip 28. Finally, Dalal was cited for its teaching of an IR heat source and for application of its method to wafers. However, Dalal's lone reference to a wafer is the statement that chip 42 could be a wafer. All of Dalal's teaching other than this passing reference is directed to mounting a chip on an interposer, not a wafer. In sum, Applicant respectfully submits that the skilled artisan would receive no motivation from these references to form the aggregate of teachings proposed by the Examiner and described in Claim 14.

Note also that Claim 14 has been amended to include the feature of "applying radiant energy to a second surface of said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing the solder balls to reach a liquid state." None of the cited references teach such a step, so even assuming for the sake of argument that a motivation for combining the references existed, the combination fails to teach or suggest all of the claim elements. Therefore, Applicant respectfully submits that Claim 14 is patentable over the cited combination of references.

Claim 15 has also been amended such that it includes the feature of "applying radiant energy having a wavelength of 0.8 to 2.8 μm to a second surface of said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing said solder balls to reach a liquid state." Support for this amendment to Claims 14 and 15 is found on page 6 of the specification at lines 26 and 27, as well as in Figures 6, 8, and 13. As discussed above, the combined references fail to teach or suggest such a step. Therefore, Applicant respectfully submits that Claim 15 is patentable over the cited combination. In addition, Claim 20 depends from Claim 15 and includes the feature of "preheating said interposer prior to alignment with the wafer." As indicated above, the skilled artisan would receive no motivation from the prior art for the combination of DiStefano's teachings with the other cited references to arrive at the claimed invention.

Claim 16 has been amended to provide a description of the relative spacings of the chip bond pads and the conductive fibers in the adhesive layer. As shown in Figure 12 of the instant specification, the conductive fibers exist throughout the breadth of the adhesive layer (or at least throughout the region of the adhesive layer where contacts are expected to be made), including at points between the locations of the bond pads. In contrast, Arima's through-holes or vias exist in a one-to-one relation to the bond pads. The remaining cited references do not cure this deficiency of Arima. The Examiner's reference to Arima's teaching of the use of conductive paste is not relevant. The use of paste certainly does not presuppose the use of conductive fibers with that paste. Therefore, Applicant respectfully submits that Claim 16 is patentable over the cited references.

Claims 17 and 18 depend from Claims 14, 15, and 16, and are therefore patentable for at least the reasons presented above for those claims.

The Office Action contained no reasons for the rejection of Claim 19. Claim 19 depends from Claim 14 and includes the feature wherein "said step of applying radiant energy to said interposer heats said interposer to a temperature in the range of 75 to 80 percent of the temperature that causes said solder balls to reach a liquid state." As indicated in Applicant's response to the last Office Action, none of the references teach or suggest such a feature. Therefore, Applicants respectfully submit that Claim 19 is patentable over the combination of those references.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 14-20. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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Version with Markings to Show Changes Mad

In th Claim :

Please amend the claims as follows:

14. (Three times amended) A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips on a first surface of said wafer, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

forming a planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, said conductive paths forming electrical entry and exit ports on said insulating interposer;

applying radiant energy to said interposer and then aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying radiant energy to a second surface of said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing the solder balls to reach a liquid state;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports; and

separating the resulting composite structure into discrete chips.

15. (Three times amended) A method for the fabrication of a semiconductor assembly comprising:

providing a silicon semiconductor wafer comprising a plurality of undivided integrated circuit chips on a first surface of said wafer, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

forming a first planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, said conductive paths forming electrical entry and exit ports on said insulating interposer;

aligning said interposer with said solder balls [ball] so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying radiant energy having a wavelength of 0.8 to 2.8 μm to a second surface of said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing said solder balls to reach a liquid state;

said wavelength causing the wafer to heat more rapidly than said interposer;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

forming a second planar array of solder balls attached to said exit ports of said interposer so that each of said exit ports is contacted by one of said solder balls; and

separating the resulting composite structure into discrete chips.

16. (Three times amended) A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads

as electrical entry and exit ports, said contact pads arranged at a first spacing pitch;

providing an adhesive layer adjacent said wafer, said adhesive layer having first and second opposite surfaces and a multitude of electrically conductive fibers extending through electrically nonconductive material from said first surface to said second surface of the layer while remaining insulated from adjacent fibers, said fibers arranged in said adhesive layer at a second spacing pitch, said second pitch being smaller than said first pitch;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, said conductive paths forming electrical entry and exit ports on said insulating interposer;

placing said interposer vertically and in contact with said adhesive substrate;

providing a polymer film having a plurality of discrete adhesive areas;

providing a plurality of solder balls, one of said solder balls being placed on each of said adhesive areas;

aligning said polymer film to said interposer so that each of said solder balls is placed into alignment with one of said ports;

placing said solder balls in contact with said ports;

applying radiant energy to said semiconductor wafer such that said wafer uniformly increases in temperature and transfers heat to said adhesive substrate, said interposer and said solder balls, causing said solder balls to reach a liquid state;

separately controlling the temperature of said interposer in order to minimize differences in thermal expansion;

removing said energy such that all said contacts form physical bonds and said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

removing said polymer film; and

separating the resulting composite structure into discrete chips.